

RH

(19)



JAPANESE PATENT OFFICE

PATENT ABSTRACTS OF JAPAN

(11) Publication number: 2000311870 A

(43) Date of publication of application: 07.11.00

(51) Int. Cl

H01L 21/28

G03F 7/004

G03F 7/20

H01L 21/265

H01L 21/027

H01L 21/3065

H01L 21/3213

H01L 21/8238

H01L 27/092

H01L 27/08

(21) Application number: 11121408

(71) Applicant: MITSUBISHI ELECTRIC CORP

(22) Date of filing: 28.04.99

(72) Inventor: KUNIKIYO TATSUYA

(54) MANUFACTURE OF SEMICONDUCTOR DEVICE

(57) Abstract:

PROBLEM TO BE SOLVED: To realize a manufacturing method of a semiconductor device, which suppresses the width of tapering generated on the sidewalls of a resist, and enables accurate lithography.

SOLUTION: This manufacturing method of a semiconductor device comprises a process, wherein an aperture formed in a prescribed pattern is provided on a semiconductor substrate 1 and a resist mask 3b formed with a tapered part is formed on the sidewall of this aperture, a process where a water-soluble resist film 9, which is turned into a nonwater-soluble resist film when being reacted with an acid is formed on the mask 3b, a process where the film 9 and an acid are made to react with each other to form a nonwater-soluble site 9a on the tapered part, a process where the site 9a is left to remove a water-soluble resist film 9b, whereby a resist mask consisting of the site 9a formed on the tapered part and the mask 3b is formed, and a process where impurities are

implanted from the upper part of this resist mask into the substrate 1 to form an impurity region in the substrate 1.

COPYRIGHT: (C)2000,JPO

